EDP-AM-CO1 Communications Module User Manual

This document contains information on the CO1 communications IO module for the RS EDP system.

Version v5.0, 10/06/2010

Contents

1. Communications Module EDP-AM-C01

This module allows the easy interfacing to the following communication devices present on the CM:

Comms Type	Channel No.	Connector	Name	Comment
RS232	ASC0	9D Male	J305	
	ASC0	5x2 Header	P302	
RS232	ASC1	5x2 Header	P301	p3 = RX, p5 = TX
RS485	ASC1	5x2 Header	P301	p3 = RX, p5 = TX
USB device	USB DEV	USB mini socket	P303	Where available on CM
CAN	CAN CNTRL	9D Female	P201	120R on baseboard
CAN	CAN CNTRL	5x2 Header	P204	Opto-isolated CAN
CAN	CAN1	5x2 Header	P204	Opto-isolated CAN

It also carries a PCF8583 real time clock device on the I2C bus and 240 bytes of non-volatile data storage, powered from the optional lithium battery on the EDP baseboard.

Note: Only one communications module may be fitted to a baseboard at any one time.

1.1 Controller Area Network Interfaces - CAN

The first CAN channel (CAN0) from the CM (where available) is routed through the 9-D female connector as CAN-High and CAN-Low signals, ready for interfacing to an existing CAN network. CAN0 may also be routed through a galvanically isolated CAN physical layer, emerging on P204 and selectable via P205. If this is required, CAN0 TX and RX connections to the CPU on the CM must be isolated via jumpers on the CM itself (please refer to the user manual for the CM fitted). The isolated physical layer has its own 5V DC-DC convertor so that the EDP system can float relative to other CAN devices.

If the CM has a second CAN channel (CAN1), this can also be routed through the galvanically isolated CAN physical layer via P205.

An optional 120R CAN terminating resistor can be added via solder bridge J203.

1.2 Serial Interfaces

1.2.1 RS232 Interfaces

Asynchronous serial channel 0 from the CPU appears as RS232-level signals on the J305 9-D connector. To allow the RS232 connector be mounted away from the EDP hardware, the same signals are available on P302. A simple PC-style IDC 9D connector on a ribbon cable can be used.

For CMs that have a second asynchronous port, it can be routed to P301 where a PC-style IDC 9-D with ribbon cable can be used. Alternatively it can be connected to an RS485 transceiver via jumpers J302 and J303.

1.2.2 RS485

RS485 communications are supported using a Linear Technology LTC485. To make use of this option, the CM software must operate the Receive Enable/Data Enable control line. In RS485 installations where no load resistor is present, J306 allows a default one to be made available.

1.3 USB Interface

The AM unit provides support for USB 'Device' class only and does not provide any support for 'Host' class. The AM board provides a physical layer transient surge arrestor designed specifically to work with high speeds found in USB communication. The USB interface works with those CMs that have a USB peripheral on board that has been mapped to the RS-EDP backplane USB bus signals.

1.4 Real Time Clock IC

The AM module is fitted with an I2C based Real Time Calendar Clock IC. The device has an on board 32KHx watch crystal that maintains real time clock information. The device can be battery backed up via a battery fitted to the Base Board. Interfacing to this device is done via the CNTRL_I2C signals. All of the CMs currently designed are able to communicate to this device with this interface.
A set of software drivers is provided for each of the CM to allow easy access to this device. A driver library provides software support for setting up sand configuring the RTC clock, as well as displaying the information etc.

2. User Jumpers And Connectors

User-configurable jumpers

P205 – Isolated CAN traffic selector

P205 1-3	CAN0TX TTL traffic is routed to the isolated CAN transceiver
P205 3-5	CAN1TX TTL traffic is routed to the isolated CAN transceiver
P205 4-6	CAN0RX TTL traffic is routed from the isolated CAN transceiver
P205 2-4	CAN1RX TTL traffic is routed from the isolated CAN transceiver

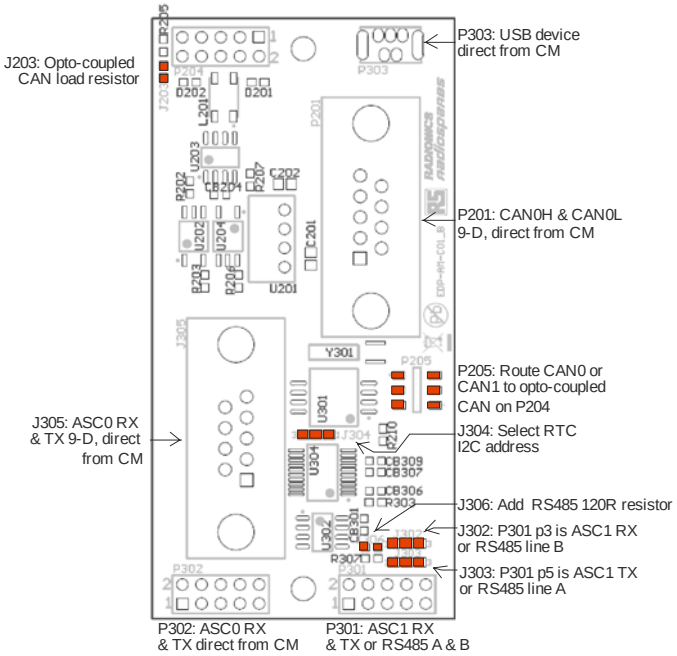
J302 & J303 Jumper Options – ASC1 - RS232/RS485 Selector

J302 2-3	ASC1 output is RS232 Rx Signal
J302 1-2	ASC1 output is RS485 B Signal
J303 2-3	ASC1 output isRS232 Tx Signal
J303 1-2	ASC1 output is RS485 A Signal

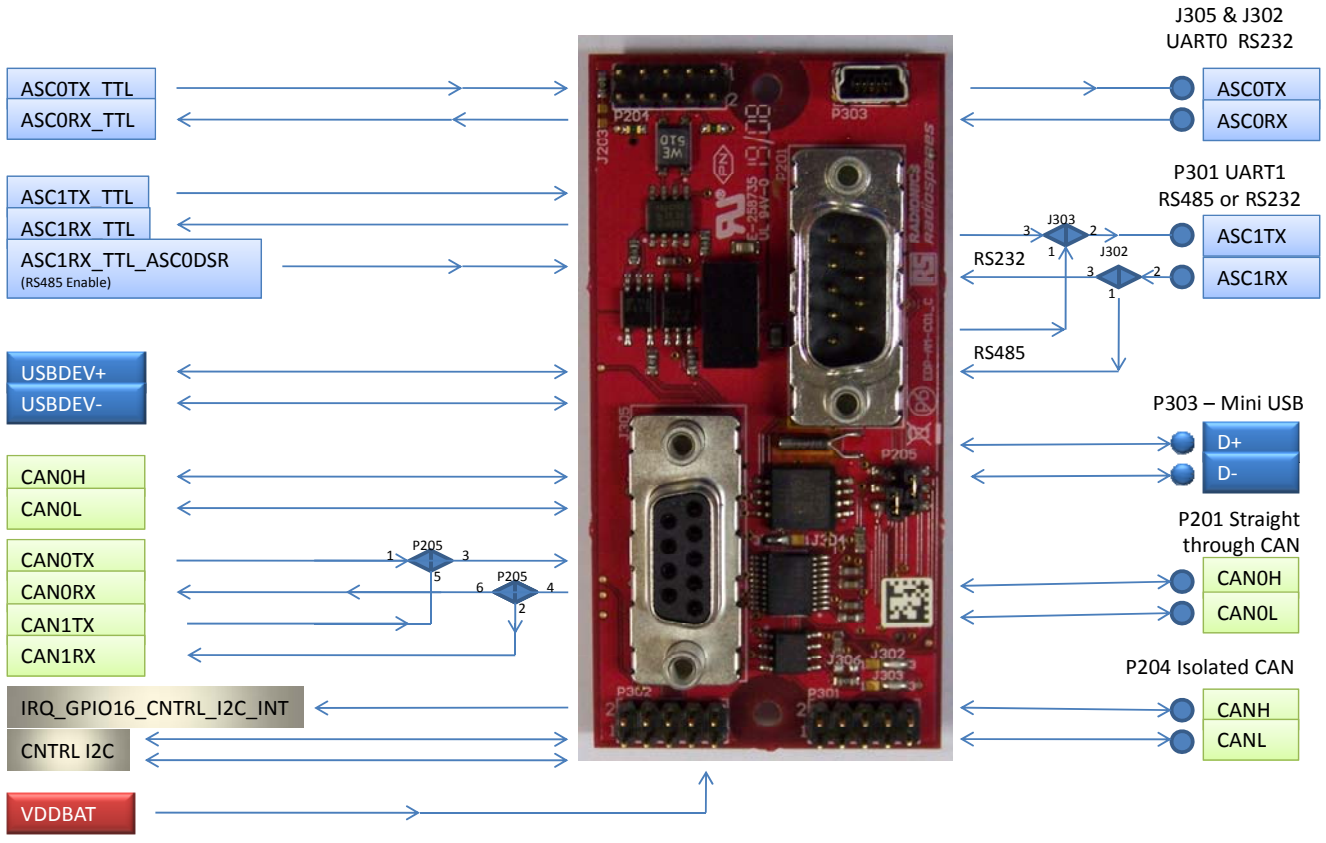
J304 – Real Time Clock Address Select

J304 1-2	A0 I2C Slave Address line is set high
J304 2-3	A0 I2C Slave Address line is set low (Default)

Changing the RTC salve I2C address may be required if there are other I2C devices in the system that shares the same I2C address. Refer to the data sheet for the PCF8583T for the I2C address settings.



CO1 - Communications Module to RS-EDP Backplane



Mapping of the Communications module to the backplane

The TTL levels for ASC0 are converted in to RS232 levels by the level shifter on the CO1 AM. The output of this serial channel is on the 9 way D connector.

The ASC1 TTL levels can be converted to either RS232 levels or RS485 levels by selecting the appropriate jumpers. To use RS485 successfully an additional third control signal is required. This is

because RS485 is half duplex and hence it cannot transit whilst receiving. To control the flow a third signal is required which is bought in from the backplane called ASC1RX_TTL_ASC0DSR.
Not all of the CPU Modules provide support for this signal, so please check with the CM to see if this signal is made available. The output of this serial ASC1 channel is available on the P301 connector. The user should connect a D connector to this, wired for RS232 or RS485 appropriately. Note: RS485 and RS232 have different pinning arrangement on the 9 way D connector, so check on-line for the correct pin out for this.

The USB Device signals USBDEV+ and USBDEV- from the backplane pass through a transient suppressor before exiting the RS-EDP system via a min USB connector P303.

Most of the CPU modules that support CAN have a local CAN transceiver on board, and hence provide the option to supply either the TTL levels CAN0TX & CAN0RX or the physical layer signals CANH and CANL. The CANH & CANL physical layer signals are routed directly onto the 9 way D connector on the Communications Module. For normal operation the user would use the local CAN transceiver on the CM and then route the physical layer CANH and CANL signals down the backplane. The physical layer CAN traffic is then accessed via the 9 way D connector on the Communication Module.

If the user would like isolated CAN traffic then the user would normally set up the Command CPU Module to output TTL level CAN traffic, CAN0TX and CAN0RX instead. This TTL level traffic is then routed via jumper on the Communications Module to a physical layer device which is electrically isolated from the RS-EDP system. This floating CAN output is available on the P204 connector which the user can then attach a 9 way D connector in the normal fashion to access the traffic.

In situations where the main CPU module has two CAN channels then the first CAN channel CAN0 is set up for use with the local CAN transceiver on the CM. This will provide the CAN0H and CAN0L physical layer signals that will appear on the 9 way D connector on the Communications Modules.

The second channel will be set up to output TTL level traffic on CAN1Rx and CAN1TX. This traffic is then routed via the backplane to the Communications module where it is then selected via jumper to enter the isolation circuit and physical layer CAN transceiver. CAN1 isolated physical layer traffic is therefore available on P204.

The AM also has on board a Real time clock device which is supported during power down by a battery on the Base Board. The RTC can be accessed via the CNTRL_I2C I2C bus. The AM also provides an interrupt line to the MCU to provide wake up etc from RTC alarm events etc.

2.1 Mapping Of CPU Pins To The Communications Module

The connectors on the Communications Module are connected to the CPU module as shown below. Only two examples are shown, one for the STR9 module and one for the XC167 module.

Please note that the USB device connector is inactive when the XC167 module is fitted and that that the second serial port is not available when the Ethernet PHY is enabled on the STR9 module.

Finally, there is no second CAN channel available with the STR9 as the MCU does not have a second CAN peripheral. Each of the CMs are different in capability and hence not all of the resource on the AMs is available to all CMs.

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-CO1 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
P3.2	P5.6	IRQ_GPIO16_CNTRL I2C INT
Digital GND	Digital GND	Digital GND
86 CAN0 TX	NC	CAN1 TX
85 CAN0 RX	NC	CAN1 RX
60 RxD1	P1.1 (PHY Disabled)	ASC1 TX TTL
P20.2	P3.1	ASC1 RX TTL_ASC0 DSR
59 TxD1	P1.0 (PHY Disabled)	ASC1 RX TTL
69 TxD0	P5.0	ASC0 TX TTL
70 RxD0	P5.1	ASC0 RX TTL
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-CO1 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
Digital GND	Digital GND	Digital GND
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
3V3 Vbatt	3V3 Vbatt	3V3 Vbatt
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-CO1 Allocation
Vcc 5V from reg	Vcc 5V from reg	Vcc 5V from reg
Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU
Vcc 3V3 from reg	Vcc 3V3 from reg	Vcc 3V3 from reg
NC	USBDN	USB DEV D+
NC	USBDP	USB DEV D-
Digital GND	Digital GND	Digital GND
25 SDA2	P2.1	CNTRL I2C SDA
26 SCL2	P2.0	CNTRL I2C SCL
CANL0	CANL0	CANL0
CANH0	CANH0	CANH0
87 CAN1 TX	P3.2	CAN0 TX
84 CAN1 RX	P3.3	CAN0 RX

3. Software Support

The Communication Module is supported with the appropriate driver software for the respective CM. As there are several CPU Modules each with its own CPU type there exists many versions of the software to exercise the Communication Module. The software provides a supported library for CAN where appropriate, the Real Time Clock set up and configuration, and the UART drivers. Support for the USB is not currently.

Module Position 1

EDPCON1 IO Connector

J101

AN_REF	1	2	
AN0	3	4	AN1
AN2	5	6	AN3
AN4	7	8	AN5
AN6	9	10	AN7
AN8	11	12	AN9
AN10	13	14	AN11
AN12	15	16	AN13
AN14	17	18	AN15
VAGND	19	20	VAGND
GPIO0	21	22	GPIO1
GPIO2_MCIDAT0	23	24	GPIO3
GPIO4_MCIDAT1	25	26	GPIO5_I2STX_WS
GPIO6_MCIDAT2	27	28	GPIO7_I2SRX_CLK
GPIO8_MCIDAT3	29	30	GPIO9_I2SRX_WS
GPIO10_MCICLK	31	32	GPIO11_I2SRX_SDA
GPIO12_MCICMD	33	34	GPIO13_I2STX_CLK
GPIO14_MCIPWR	35	36	GPIO15_I2STX_SDA
IRQ_GPIO16_CNTRL I2C INT	37	38	CPU DACO0_GPIO17
IRQ_GPIO18_I2C GEN0 INT	39	40	CPU DACO1_GPIO19
IRQ_GPIO20_I2C GEN1 INT	41	42	EVM0_GPIO21
IRQ_GPIO22_I2C INT	43	44	EVM1_GPIO23
GPIO24_AD7	45	46	GPIO25_AD15
GPIO26_AD6	47	48	GPIO27_AD14
GPIO28_AD5	49	50	GPIO29_AD13
GPIO30_AD4	51	52	GPIO31_AD12
GPIO32_AD3	53	54	GPIO33_AD11
GPIO34_AD2	55	56	GPIO35_AD10
GPIO36_AD1	57	58	GPIO37_AD9
GPIO38_AD0	59	60	GPIO39_AD8
EVG0_GPIO40	61	62	EVM2_GPIO41_CAPADC
EVG1_GPIO42	63	64	EVM3_GPIO43
EVG2_GPIO44	65	66	EVM4_GPIO45
EVG3_GPIO46	67	68	EVM5_GPIO47
EVG4_GPIO48	69	70	EVM6_GPIO49
EVG5_GPIO50	71	72	EVM7_GPIO51
EVG6_GPIO52	73	74	EVM8_GPIO53
EVG7_GPIO54	75	76	EVM9_GPIO55
EVG8_GPIO56	77	78	EVG9_GPIO57
EVG10_GPIO58	79	80	EVG11_GPIO59
EVG12_GPIO60	81	82	EVG13_GPIO61
EVG14_GPIO62	83	84	EVG15_GPIO63
EVG16_GPIO64	85	86	EVG17_GPIO65
EVG18_GPIO66	87	88	EVG19_GPIO67
ASC0 RX TTL	89	90	EVM10_GPIO68_ASC0 CTS
ASC0 TX TTL	91	92	EVG20_GPIO69_ASC0 RTS
ASC1 RX TTL	93	94	SPI_SSC MRST_MISO
ASC1 TX TTL	95	96	SPI_SSC MTSR_MOSI
ASC1 TX TTL_ASC0 DTR	97	98	SPI_SSC CLK
ASC1 RX TTL_ASC0 DSR	99	100	MOTOR P0L
SPI_SSC #CS_NSS	101	102	MOTOR P0H
ETH TX+	103	104	MOTOR P1L
ETH TX-	105	106	MOTOR P1H
ETH RX+	107	108	MOTOR P2L
ETH RX-	109	110	MOTOR P2H
ETH LNK LED	111	112	MOTOR PWM
ETH RX LED	113	114	EMG TRP
ETH SPD LED	115	116	MOTOR H0_ENC0
I2C GEN1 SDA	117	118	MOTOR H1_ENC1
I2C GEN1 SCL	119	120	MOTOR H2_ENC2
CAN1 RX	121	122	MOTOR TCO FB
CAN1 TX	123	124	+3V3BAT
VCC_CM	125	126	VCC_CM
+3V3	127	128	+3V3
+5V	129	130	+5V
SGND	131	132	SGND
+12V	133	134	+12V
+12V	135	136	+12V
12VGND	137	138	12VGND
12VGND	139	140	12VGND

Tyco Amp 140 Way

EDPCON2 Bus/Control Connector

J102

#RESIN	1	2	#RESIN
#RESOUT	3	4	#RESOUT
I2C GEN0 SDA	5	6	I2C GEN0 SDA
I2C GEN0 SCL	7	8	I2C GEN0 SCL
SGND	9	10	SGND
A15_AD15	11	12	A15_AD15
A14_AD14	13	14	A14_AD14
A13_AD13	15	16	A13_AD13
A12_AD12	17	18	A12_AD12
A11_AD11	19	20	A11_AD11
A10_AD10	21	22	A10_AD10
A9_AD9	23	24	A9_AD9
A8_AD8	25	26	A8_AD8
A7_AD7	27	28	A7_AD7
A6_AD6	29	30	A6_AD6
A5_AD5	31	32	A5_AD5
A4_AD4	33	34	A4_AD4
A3_AD3	35	36	A3_AD3
A2_AD2	37	38	A2_AD2
A1_AD1	39	40	A1_AD1
A0_AD0	41	42	A0_AD0
ALE	43	44	ALE
#RD	45	46	#RD
#WR	47	48	#WR
#WRH	49	50	#WRH
#PSEN	51	52	#PSEN
#CS0	53	54	#CS0
#CS1	55	56	#CS1
#CS2	57	58	#CS2
#CS3	59	60	#CS3
CAN0 RX	61	62	CAN0 RX
CAN0 TX	63	64	CAN0 TX
USB DEBUG D+	65	66	USB DEBUG D+
USB DEBUG D-	67	68	USB DEBUG D-
CNTRL SPI CLK	69	70	CNTRL SPI CLK
CNTRL SPI MRST	71	72	CNTRL SPI MRST
CNTRL SPI MTSR	73	74	CNTRL SPI MTSR
CNTRL SPI #CS_NSS	75	76	CNTRL SPI #CS_NSS
CNTRL I2C SDA	77	78	CNTRL I2C SDA
CNTRL I2C SCL	79	80	CNTRL I2C SCL
USB HOST D+	81	82	USB HOST D+
USB HOST D-	83	84	USB HOST D-
USB DEV D+	85	86	USB DEV D+
USB DEV D-	87	88	USB DEV D-
CANH0	89	90	CANH0
CANL0	91	92	CANL0
VCC_CM	93	94	VCC_CM
+3V3	95	96	+3V3
+5V	97	98	+5V
SGND	99	100	SGND

Tyco Amp 100 Way

Checked By:	Title: *EDP Connectors*		*Hitex (UK) Ltd.*
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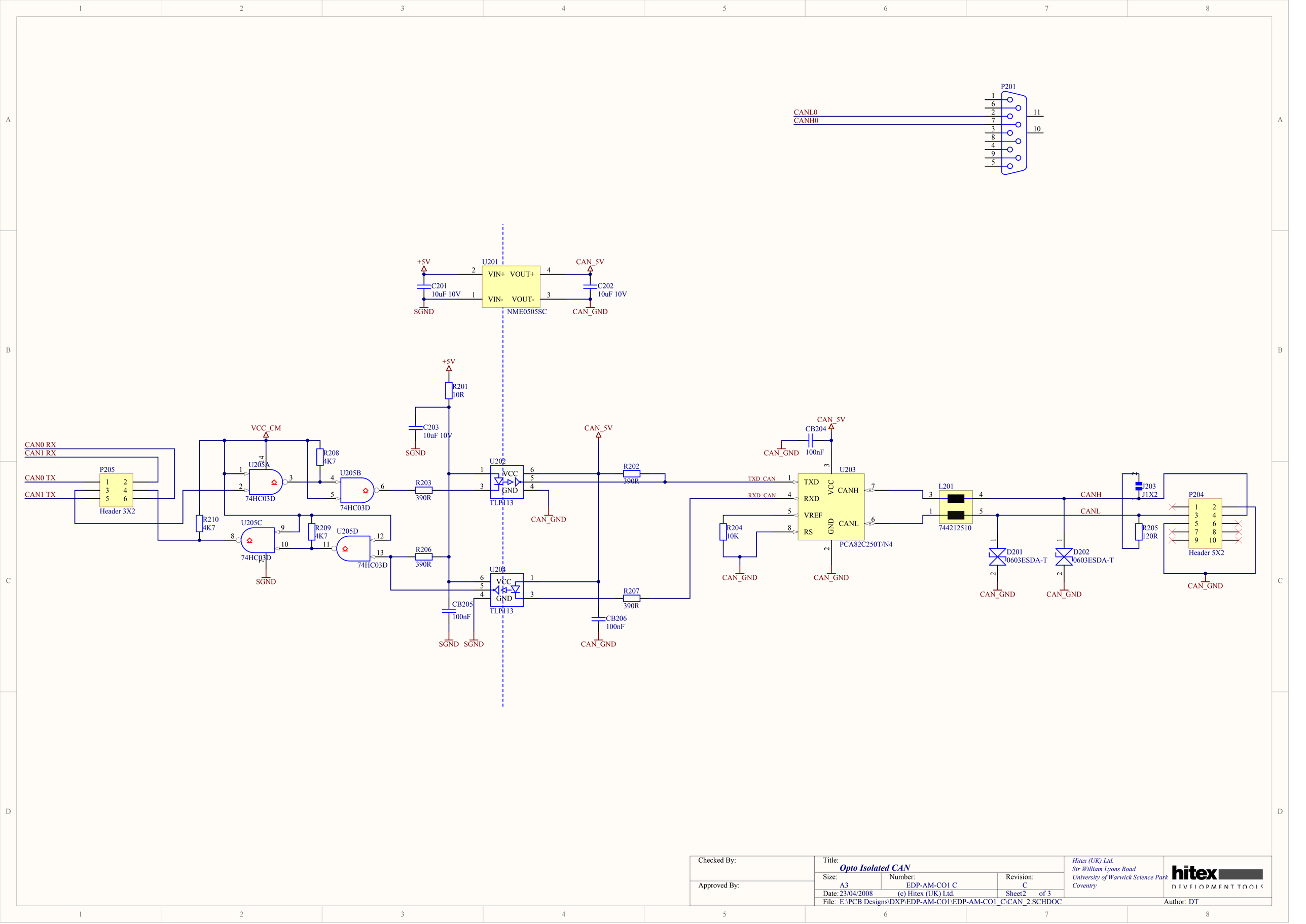

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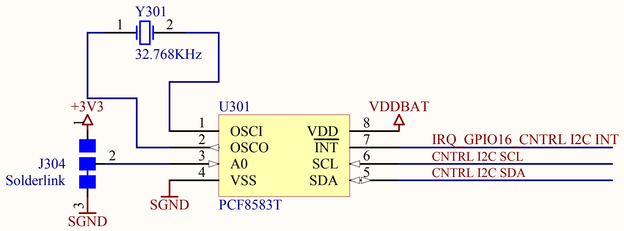

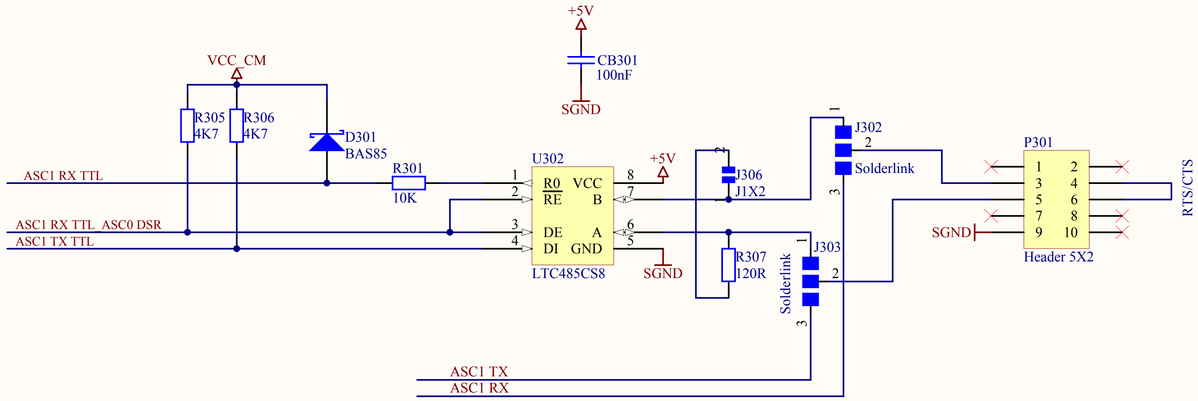

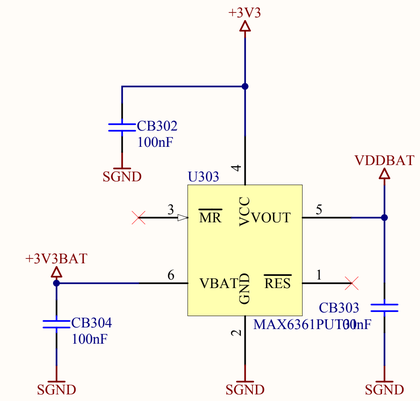

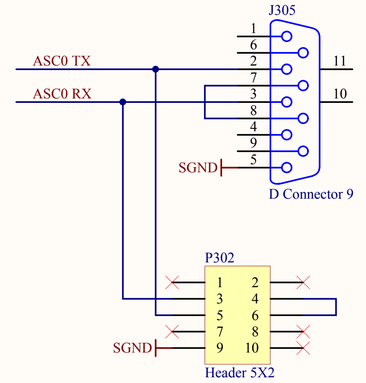

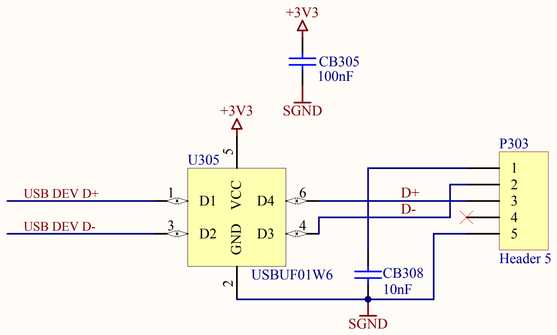

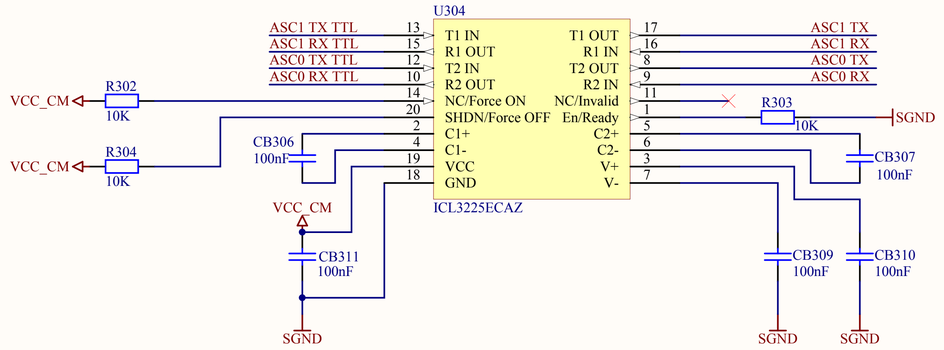

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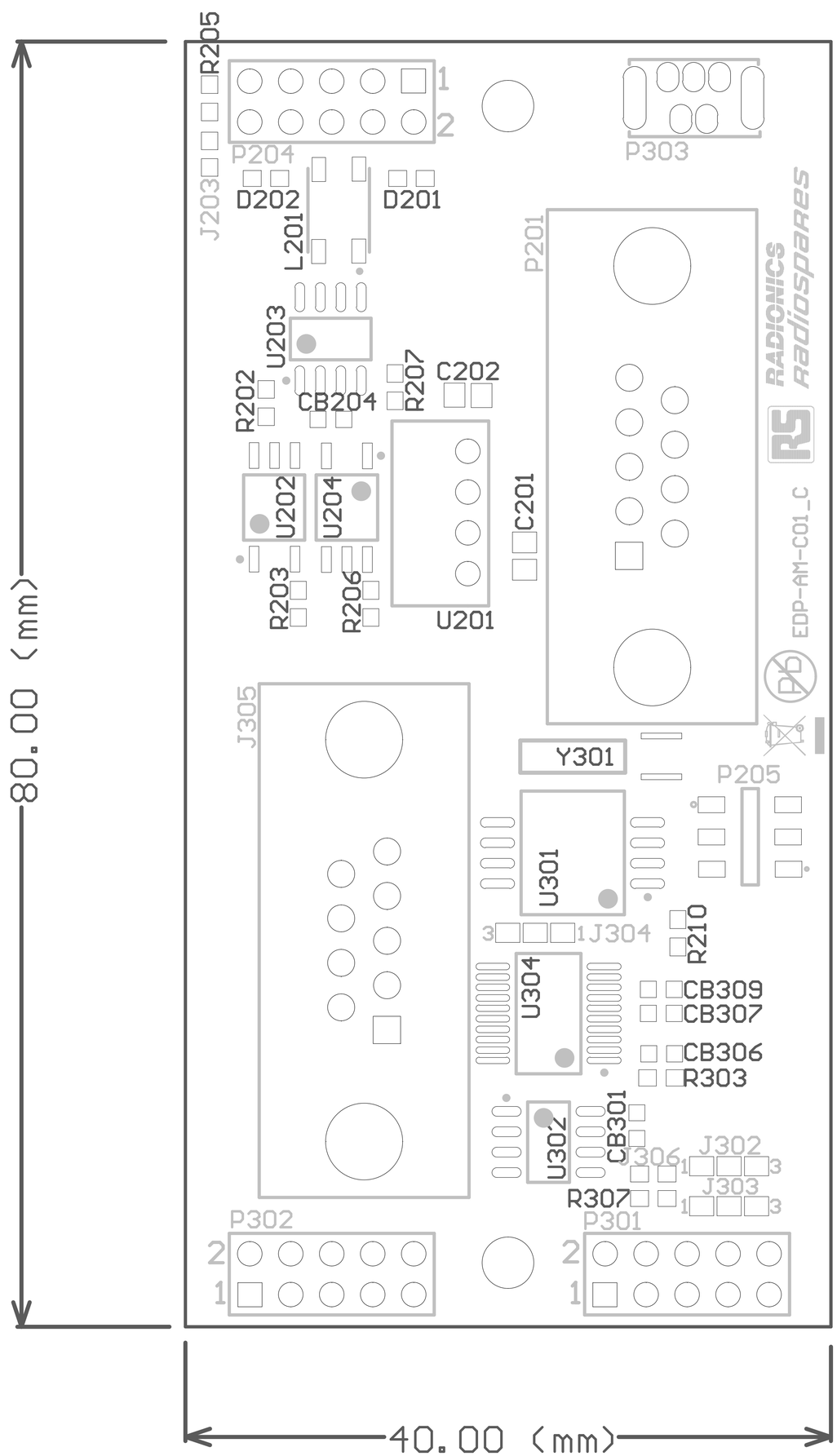
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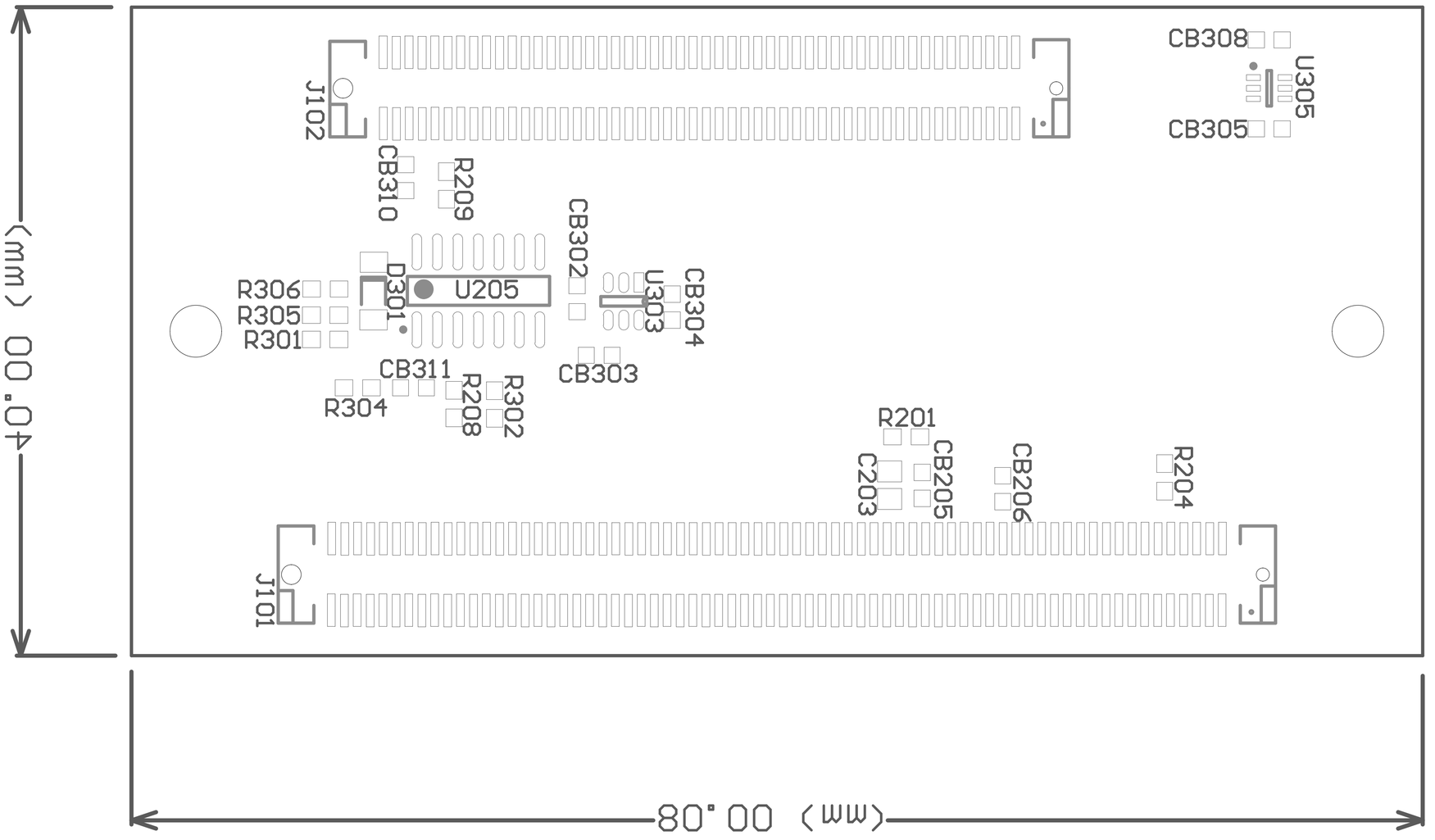
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